R[1:0]

F[2:0]]

LoadB

LoadA

CLK

Execute

Control Unit

D[3:0]

Routing Unit

1-bit wide

Arithmetic Logic Unit

Shift Register A

Shift Register B

A[0]

A[0]

F(A,B)

A\*

B[0]

B\*

B[0]

4

LED A

4

LED B

LS[3:0]]

A[3:0]

B[3:0]

CLK

LoadB

LoadA

D[3:0]

R[1:0]

F[2:0]]

Execute

4-bit Logic Processor

A[3:0]

B[3:0]

LED A

LED B

Shape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with low confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

B2

B3

B0

B1

A1

A3

A2

A0

CLK

D[3:0]

CLR

CLR

D[3:0]

CLK

Shift Register B

Shift Register A

A\*

SL Din (Not Used)

LSA1

LSA0

B\*

SL Din (Not Used)

LSB1

LSB0

R0

R1

R1

R0

R0

R1

A

B

A

F(A,B)

A\*

A

B

F(A,B)

B

B\*

B\*

A\*

A

F(A,B)

B

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

F2

F1

B

A

F0

Vcc

B

A

A

B

A

B

F2

F0

F(A,B)

F1

A picture containing timeline

Description automatically generated

GND

Vcc

CLK

E

R0

R1

F0

F1

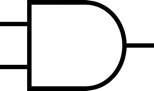
F2

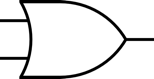
D2

D3

D1

D0

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

Vcc

B

F(A,B)

F0

F2

A

B

F1

F0

F2

A

B

A

A

B

F1

LSB

LSA

LSB1

LSA1

LSB0

CLK

LoadB

LoadA

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

E

C0

C1

S

Execute(E)

Vcc

ENT

ENP

4-bit Binary Counter

Shape

Description automatically generated with medium confidence

CLK

E

C1

C1

C0

C0

CLK

S

S

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated

S

LSA0

LSA

E

LoadA

LSA0

Shape

Description automatically generatedShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

LoadB

E

LSB

LSB0

S

Shape

Description automatically generated with medium confidence

LSB

LSA

LSA0

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

Execute(E)

S

LSA1

Shape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidenceShape

Description automatically generated with medium confidence

C1

C1

Vcc

4-bit Binary Counter

LSB1

LoadA

C0

C0

CLK

CLK

ENT

ENP

Shape

Description automatically generated with medium confidence

LSA

S

LSA0

S

S

A picture containing venn diagram

Description automatically generated

E

LoadB

A picture containing venn diagram

Description automatically generated

LoadA

A picture containing venn diagram

Description automatically generatedA picture containing venn diagram

Description automatically generatedShape

Description automatically generated with medium confidence

S

LSB

LSB0

E

LSB0

LoadB

CLK

Arc Label

Input/Output => count/execute/shift

01/d/1

10/d/1

11/d/1

00/1/0

00/1/1

00/0/0

B[3:0]

A[3:0]

LoadA

LoadB

CLK

D[3:0]

R[1:0]

F[2:0]]

Execute

4-bit Logic Processor